PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P 001 407 PC	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/EP 02/07699	International filing date *(day/month/year)* 10.07.2002	Priority date *(day/month/year)* 10.07.2002
International Patent Classification (IPC) or both national classification and IPC H04L12/64		
Applicant TELEFONAKTIEBOLAGET L.M. ERICSSON et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 6 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
22.01.2004	11.11.2004
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Lastoria, G Telephone No. +49 89 2399-7339

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/EP 02/07699

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-17 as originally filed

Claims, Numbers

1-21 received on 13.08.2004 with letter of 13.08.2004

Drawings, Sheets

1/4-4/4 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).

   ☐ the language of publication of the international application (under Rule 48.3(b)).

   ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐ contained in the international application in written form.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority in written form.

   ☐ furnished subsequently to this Authority in computer readable form.

   ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   ☐ the description, pages:

   ☐ the claims, Nos.:

   ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-21
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-21
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-21
	No:	Claims	

2. Citations and explanations

   see separate sheet

1. **Re Item V**

1.1 References made to the following documents:

D1: WO 99/65196 A (MERLOT COMMUNICATIONS INC ;SETARO JOSEPH (US); EVANS PATRICK A (US) 16 December 1999 (1999-12-16)

2. **Reasoned statement under Article 35(2) PCT with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

2.1 **Object**: The present application relates to a data transmission link (**claim 1**), a method (**independent claim 9**) and a node (**independent claim 15**) for transmitting time-sensitive data between a first node and a plurality of end nodes, the nodes being connected by a broadband packet-switched network.

2.2 **Prior Art**: Document D1 represents the closest state of the art. It describes a local area network (LAN) adapted for packet switching of standard Ethernet packets, said LAN employing a communication switching module to control flow of both time-sensitive and non-time-sensitive data. User Terminal Equipment (UTE) adapters are connected to both devices generating said time-sensitive and non-time-sensitive data. Furthermore, a master oscillator in the communication switching module synchronises the devices on the LAN through fixed rate transmission of master Ethernet packets, which serve to synchronize local clocks in the UTE adapters.

2.3 **Problem**: Hence the problem can be formulated as to enable reliable transmission of time-sensitive data obviating extensive and costly modification of the network infrastructure, such as the mentioned inclusion of adapters (UTE) to each user terminal's end devices.

2.4 **Invention**: The problem is solved by the provision of a time delay signal generator at the end nodes, said time delay signal generator being responsive to time delay information received from the first node for generating a time delay signal.

2.5 The requirements of Article 33 PCT are considered to be fulfilled because none the documents cited in the International Search Report discloses or render

obvious the claimed solution of including in the end node a time delay signal generator responsive to a time delay information sent by the first node.

3. Remarks concerning formal defects in the international application

3.1 The ultimately adopted main claims should have been drafted in the proper two-part "characterised" form recommended by Rule 6.3 (b),(I),(ii) PCT, having a preamble that correctly reflects the nearest prior art, presumably that represented by the above noted document D1.

3.2 In order to meet the requirements of Rule 5.1 (a) (ii) PCT, the most relevant prior art, i.e. the document D1 should have been acknowledged by reference and briefly discussed in the introductory part of the description, preferably in such a way that the inventive merit of what is claimed can be readily understood.

Claims:

1. A data transmission link for transmitting time-sensitive data, said link including a first node (10) connected to a plurality of end nodes (30) by a broadband packet-switched network (1), whereby each end node (30) is connected to at least one end terminal (40),
each of said end nodes (30) including:
timing generation circuitry (350, 360, 370) adapted to generate an output timing signal that is phase locked to a received reference timing signal originating at said first node (10),
means (380) for receiving data structure information from said first node (10) and identifying a data structure format from said information for transmitting time-sensitive data between said end nodes (30) and said end terminals (40),
a delay signal generator (320) for generating a delay signal in response to delay information received from said first node (10), and
data conversion means (340) communicating with said delay signal generating means (320), said data structure receiving means (380) and said timing generation circuitry (350, 360, 370), said data conversion means being arranged to receive payload data from said first node (10) and retransmit payload data identified as time-sensitive data in a synchronous manner to said end terminal, wherein the timing of said payload data transmission is adjusted in each end node on the basis of said received timing signal, said received data structure format and said received delay signal, such that all end nodes transmit said payload data substantially simultaneously.

2. A link as claimed in claim 1, wherein at least one intermediate node is arranged between said first node (10) and at least one of said end nodes (30), each said intermediate node including timing generation circuitry (50, 60) adapted to generate an output timing signal that is phase locked to a received reference timing signal originating at said first node (10), and to propagate said output timing signal to said end node (30).

3. A link as claimed in claim 1 or 2, wherein said means (310) for receiving data structure information from said first node (10) further includes means (310) for extracting a data transmission start time marker from said information, said data transmission start marker indicating an absolute start to transmit time for transmitting time-sensitive data between said end nodes (30) and said end terminals (40).

4. A link as claimed in claim 3, wherein said delay signal generator (320) is arranged to adjust the timing of said transmission start time marker by said generated delay.

5. A link as claimed in any previous claim, wherein each said end node (30) is arranged to determine a node transmission delay between said end node (30) and said first node (10) and to communicate this node transmission delay to said first node (10), and wherein said first node (10) is arranged to determine the maximum node transmission delay from each end node (30) and communicate this maximum node transmission delay to all end nodes (30) as delay information.

6. A link as claimed in claim 5, wherein said node transmission delay is the round-trip delay between and end node (30) and said first node (10).

7. A link as claimed in any previous claim, wherein said timing generation

circuitry includes means (50) for extracting a timing reference from a received signal, means (71, 72, 73; 350, 360, 370) for phase locking a generated timing signal to said timing reference and means (60) for imposing said phase locked timing signal on an output signal to generate said output timing signal.

8. A link as claimed in any previous claim, wherein said network is an Ethernet.

9. A method for transmitting time-sensitive data through a packet-switched network between a first node (10) and a plurality of end nodes (30), wherein each end node (30) is connected to at least one end terminal (40) said method including:
propagating a timing signal through said network from said first node to each said end nodes,
transmitting a signal indicative of a data structure type from the first node to each end node, said data structure type identifying the data format for transmission from said end node to said end terminals,
transmitting a delay figure from said first node to each end node, said delay figure being indicative of the maximum transmission delay between said first node and any one of said end nodes,
transmitting payload data between said first node and said end terminals, whereby the payload data transmitted between each end node and the corresponding end terminal is formatted in said identified data structure format in accordance with said timing signal and adjusted in dependence on said delay figure such that payload data transmission from each end node to each end terminal occurs substantially synchronously.

10. A method as claimed in claim 9, further including the step of generating said delay figure by determining a maximum transmission delay

between any end node and said first node.

11. A method as claimed in claim 10, further including the step of sending a delay message from an end node to said first node and returning the delay message to the end node, calculating a transmission delay based on the return time of said message, and communicating this transmission delay to said first node.

12. A method as claimed in any one of claims 9 to 11, wherein said step of transmitting a signal indicative of a data structure type includes transmitting a burst of information messages, wherein the interval between each information message is indicative of the transmission repetition rate of the identified data structure from said end node to said terminals.

13. A method as claimed in claim 12, further including the step of:
in each end node, determining the interval between each information message, generating a periodic timing marker corresponding to said interval and utilising said timing marker to commence transmission of an identified data structure of payload data to said end terminal.

14. A method as claimed in claim 13, further including the step of:
in each end node adjusting said periodic timing marker in dependence on said delay figure.

15. A node in a broadband packet-switched adapted to receive packet switched-data in a first format and transmit synchronous data in a second format, said node including
a frequency generator (360) for generating a timing signal and means (350, 370) for adjusting the phase of said timing signal to a received reference signal,

means (380, 310) for receiving data structure information and for identifying said second data format from said data structure information, and

means (340) arranged to receive said adjusted timing signal and communicating with said data structure identifying means (380) and said data structure identifying means (320, 310) for converting data received in said first format into data in said second format.

16. A node for use in a broadband packet-switched network adapted to receive packet switched-data in a first format from a sending node in said network and transmit synchronous data to an end terminal (40) located outside said network in a second format, said node (30) including

timing generation circuitry (350, 360, 370) adapted to generate an output signal timing signal that is phase locked to a received reference timing signal,

means (380) for receiving data structure information indicative of the data structure and repetition rate of said second format,

a delay signal generator (320) for generating a delay signal in response to delay information received from said first node (10), and

data conversion means (340) communicating with said delay signal generating means (320), said data structure receiving means (380) and said timing generation circuitry (350, 360, 370), said data conversion means being adapted to receive payload data in said first data format and retransmit payload data identified as time-sensitive data in said second format, wherein the timing of said payload data transmission is adjusted on the basis of said received timing signal, said received data structure format and said received delay signal.

17. A node as claimed in claim 16, further including means (320, 310, 330) for identifying start of data received in said first format, wherein said start of

data represents the start of a unit of payload data to be transmitted in said second format.

18. A node as claimed in claim 16 or 17, wherein said means (310) for receiving data structure information from said first node (10) further includes means (310) for extracting a data transmission start time marker from said information, said data transmission start marker indicating an absolute start to transmit time for transmitting time-sensitive data between said end nodes (30) and said end terminals (40).

19. A node as claimed in claim 18, wherein said delay signal generator (320) is arranged to adjust the timing of said transmission start time marker by said generated delay.

20. A node as claimed in any one of claims 16 to19, wherein said node is further adapted to determine a node transmission delay from said sending node (10)

21. A node as claimed in claim 20, wherein said node transmission delay is the round-trip delay between said node and said sending node (10).

22. A node as claimed in any one of claims 16 to 21, wherein said timing generation circuitry includes means (50) for extracting a timing reference from a received signal, means for phase locking a generated timing signal to said timing reference (61, 62, 70; 350, 360, 370) and means (60) for imposing said phase locked timing signal on an output signal to generate said output timing signal.